LA5627W



Four-Channel Switching Regulator Controller

Overview

The LA5627W is a 4-channel switching regulator controller IC.

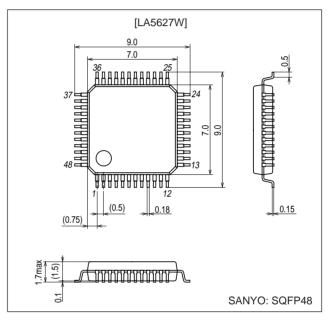
Functions and Features

- Supports low-voltage operation with a minimum operating voltage of 1.8 V (when the internal sub-power supply is not used).
- Operates from voltages as low as 1.2 V when the internal sub-power supply is used.
- Independent standby circuits in each of the four channels

Package Dimensions

unit: mm

3163B-SQFP48



Specifications Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V _{CC} max		14	V
Maximum supply voltage 2	V _{BATT} max		14	V
Allowable power dissipation	Pd max	Independent IC	0.45	W
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

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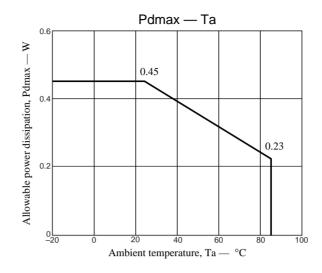
SANYO Electric Co., Ltd. Semiconductor Company TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Operating Conditions at $Ta = 25^{\circ}C$

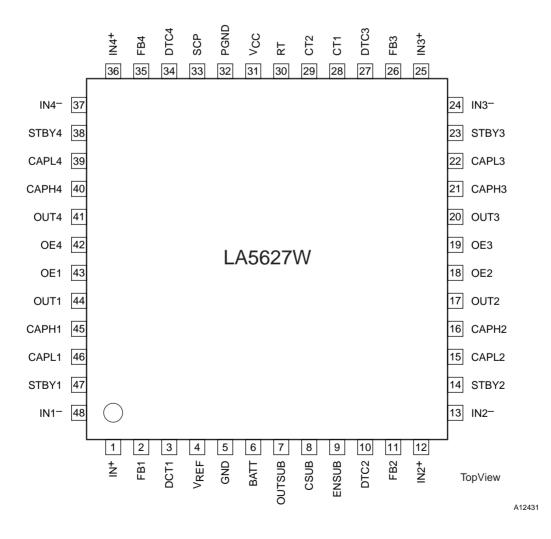
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V _{CC}		1.8 to 11	V
Supply voltage 2	VBATT		1.2 to 11	V
Output sink current	ISINK max		0 to 30	mA
Reference voltage output current	I _{REF}		0 to 1	mA
Timing resistor value	RT		3 to 30	kΩ
Timing capacitor value	СТ		100 to 1000	pF
Triangle wave frequency	fosc		0.1 to 1	MHz

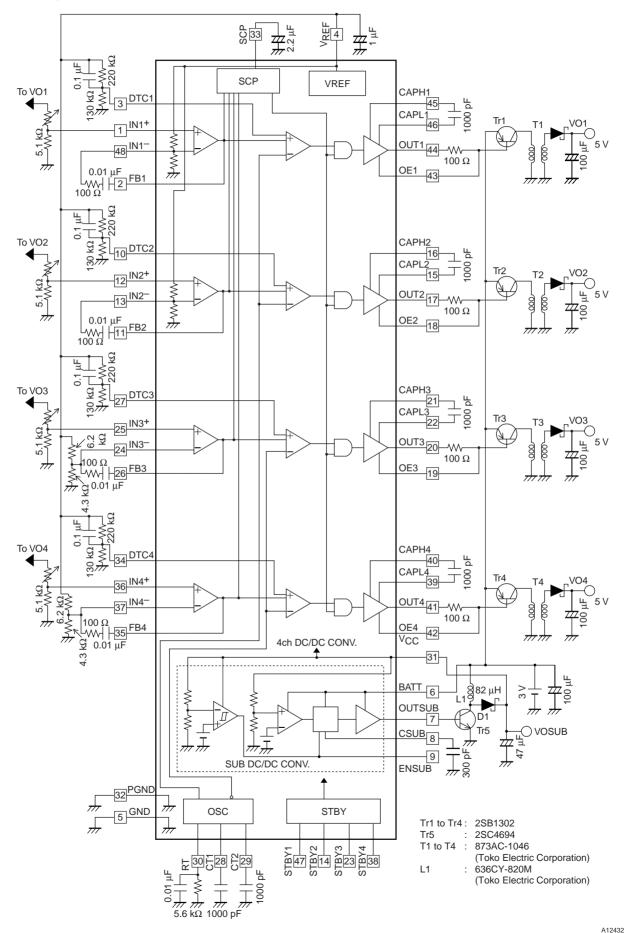
Electrical Characteristics at Ta = 25°C, V_{CC} = 3 V, VSTBY1 to 4 = 3 V

Parameter	Symbol	Conditions		Ratings		
			min	typ	max	Unit
[Error Amplifier]						
IN- pin internal bias voltage	V _{LOW} FB	IN1- and IN2- pins	0.475	0.5	0.525	V
Low-level output voltage	V _{LOW} FB	IFB = 20 μA			1	V
High-level output voltage	VHi FB	IFB = -20 μA	2.25			V
Common-mode input voltage range	V _{ICM} IN		0		2	V
[Protection Circuits]						
Threshold voltage	V _{TH} SCP		1.1	1.25	1.4	V
SCP pin current	I _O SCP			3.8		μA
[Stop Period Adjustment Block]			· · ·			
Input bias current	I _B DET		-15	-3		μA
Threshold voltage 1	V _{TH} 1 DET	Duty cycle = 100%	0.35	0.4	0.45	V
Threshold voltage 2	V _{TH} 2 DET	Duty cycle = 0%	0.67	0.77	0.87	V
[Output Block]			I			
OUT pin saturation voltage	V _{OSAT} OUT	I _{OUT} = +30 mA			0.6	V
OUT pin output voltage	V _O OE	$I_{OUT} = -3 \text{ mA}, \text{CAPH} = V_{CC}$	2			V
[Triangle Wave Oscillator Block]						
Current setting pin voltage	V _T RT	R _T = 5.6 kΩ	1.19	1.26	1.33	V
Output current	I _{OH} CT	$V_{CT} = 0.5 \text{ V}, \text{ R}_{T} = 5.6 \text{ k}\Omega$		230		μA
Output current ratio	∆l _O CT		0.8	1.0	1.2	
Oscillator frequency	f _{OSC} 1		200	260	320	kHz
[Reference Voltage Block]	1	1				
Reference voltage	V _{REF}		1.19	1.26	1.33	V
Line regulation	VLN REF	V _{CC} = 1.8 V to 11 V		10		mV
Load regulation	VLD REF	$I_0 18 = -0.1 \text{ mA to } -1 \text{ mA}$		10		mV
[Sub-Power Supply Circuit]	1	1				
VOSUB setting voltage	V _O SUB		2.1	2.2	2.3	V
OUTSUB pin source current	I _{OUT} SUB	$V_{BAT} = 1.2 \text{ V}, V_O \text{SUB} = V_{CC} = 1.8 \text{ V},$ $V_{OUT} \text{SUB} = 0.7 \text{ V}, \text{CSUB} = 0.9 \text{ V}$	1			mA
CSUB oscillator frequency	f _C SUB			100		kHz
EN comparator threshold voltage	V _{TH} ENSUB		3.0	3.1	3.2	V
EN comparator hysteresis	ΔV _{HYS} ENSUB		0.2	0.4	0.6	V
ENSUB shorted current	I _{EN} SUB				120	μA
[Standby Circuit]	1	I	I			
On voltage	V _{ON} STBY		1.15			V
Off voltage	V _{OFF} STBY				0.2	V
Pin input current	I _{IN} STBY	VSTBY = 3 V			70	μA
[All Circuits]	1	1				
Operating current drain	I _{CC} 1	ENSUB = 0 V		7.5	10.5	mA
Standby mode current drain	I _{CC} 2				10	μA



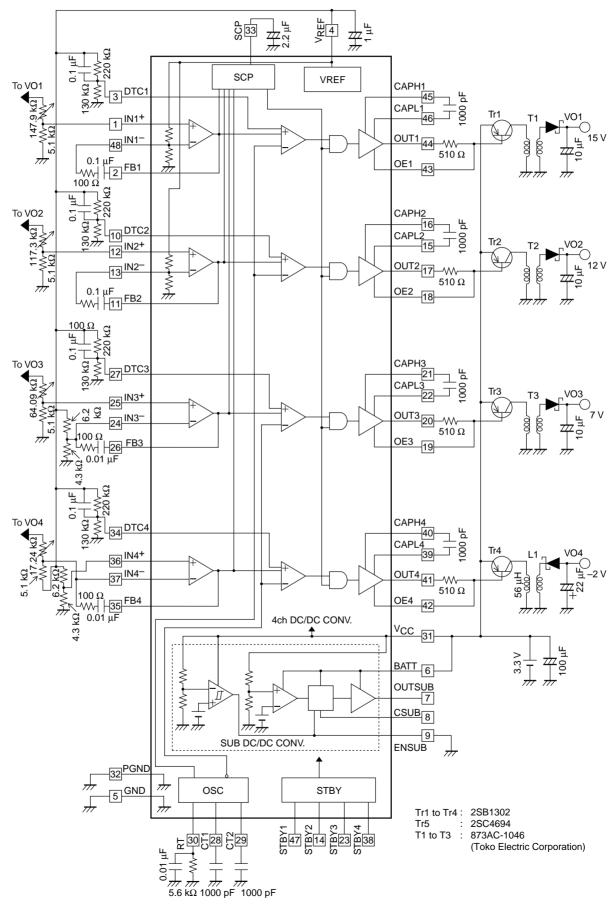
Pin Assignments





Block Diagram (Application Circuit Example 1)

Application Circuit Example 2



A12433

Relationship Between V_{BATT} and V_{CC}

Figure 1 shows the relationship between V_{BATT} and V_{CC} in the block diagram.

(Note that this applies when the forward voltage (VF) for D1 is 0.2 V and the loss in the resistive component of L1 is less than 0.2 V.)

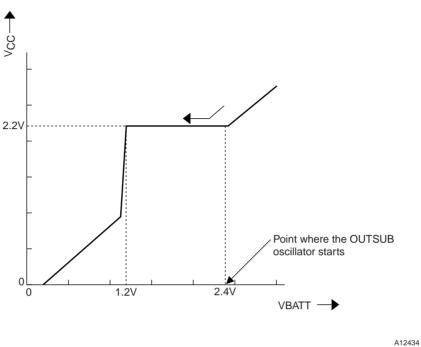


Figure 1 Relationship Between V_{BATT} and V_{CC} (The voltage values in the figure are the typical values for the device.)

When the Sub-DC/DC Converter is not Used The related pins must be connected as shown in figure 2.

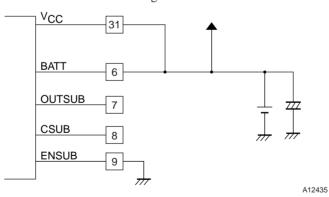


Figure 2 Peripheral Circuit when the Sub-DC/DC Converter is not Used

Notes on the Output Stage

Figure 3 shows the equivalent circuit for the output stage. The OUT pin operates as an open-collector output when the CAPL, CAPH, and OE pins are left open.

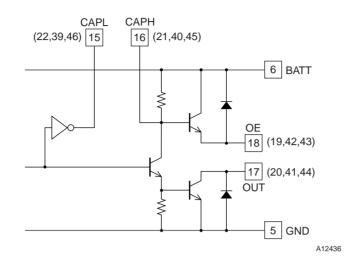
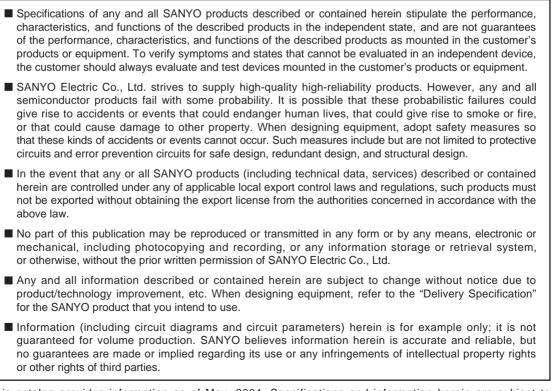


Figure 3 Output Stage Equivalent Circuit



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